P420m Half-Height and Half-Length PCIe NAND Flash SSD

MTFDGAR1T4MAX, MTFDGAR700MAX

Features

- Micron® 25nm MLC NAND Flash
- ONFI 2.1-compliant Flash interface
- PCIe Gen2 x8 host interface
- Capacity:[1] 700GB, 1.4TB
- Endurance (total bytes written)[2,3]
  - 700GB: 4.6PB (4KB random write), 9.7PB (128KB sequential write)
  - 1.4TB: 9.2PB (4KB random write), 19.5PB (128KB sequential write)
- Temperature
  - Operating: 0°C to +85°C[4]
  - Storage (in system): 0°C to +40°C[5]
  - Storage (on shelf): –40°C to +85°C[5]
  - Temperature throttling support
- ATA modes supported
  - PIO modes 3 and 4
  - Multiword DMA modes 0, 1, 2
  - Ultra DMA modes 0, 1, 2, 3, 4, 5, 6
  - ATA8-ACS2 command set support
  - ATA security feature command set and password login support
- Industry-standard 512-byte sector size support
- Full end-to-end data protection
- Native command queuing up to 256 commands
- Bootable[6]
- Power
  - 700GB: 25W RMS
  - 1.4TB: 25W RMS[7]
- Random read/write (steady state) performance[8]
  - Random read: Up to 750,000 IOPS (4KB IO size)
  - Random write: Up to 95,000 IOPS (4KB IO size)
  - Random read/write (70/30) mixed workload: Up to 220,000 IOPS (4KB IO size)
- Sequential read/write (steady state) performance[8]
  - Sequential read: Up to 3.3 GB/s (128KB IO size)
  - Sequential write: Up to 630 MB/s (128KB IO size)
- Latency (queue depth 1)[8]
  - READ latency: <100µs (MIN)
  - WRITE latency: 13µs (posted) (MIN)
- Custom drivers
  - Windows Server 2012 R2 (x86-64), Hyper-V (x86-64)
  - Windows Server 2012 (x86-64), Hyper-V (x86-64)
  - Windows Server 2008 R2 SP1 (x86-64), Hyper-V (x86-64)
  - Windows 8, 8.1 (x86-64 and x86)
  - Windows 7 (x86-64 and x86)
  - RHEL 5.5–5.10, 6.0–6.5, 7 (x86-64)
  - SLES 11 SP1, SP2, SP3 (x86-64)
  - VMware 5.0, 5.1 (x86-64)
  - VMware 5.5 (inbox driver)
  - Citrix XenServer 6.0.2, 6.1, 6.2
  - Ubuntu 12.04–12.04.4, 14.04 LTS Server (64-bit)
- Reliability
  - MTTF: 2.0 million hours
  - Static and dynamic wear leveling
  - Field-upgradable firmware
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{17} bits read
  - Power holdup protection for MLC NAND
- Micron redundant array of independent NAND (RAIN) technology
- SMART command set support
- On-chip temperature monitoring
- Mechanical/electrical
  - Half-height, half-length form factor: 68.90mm x 167.65mm x 18.71mm
  - PCIe-compliant, x8 lane PCB connector
  - Weight: 700GB – 199.59g; 1.4TB – 204.12g
  - 12V power (±8%)
- Shock (nonoperational): 400g at 2ms half-sine, 150g at 10ms half-sine
- Vibration (nonoperational): 3.1 grms 5–800Hz at 30 min/axis
- RoHS compliant

Notes:
1. User capacity: 1GB = 1 billion bytes.
2. Lifetime endurance is measured not in years, but in the number of bytes that can be written to the device.
3. Workloads are 100% writes.
4. Operating temperature is the drive case temperature as measured by the SMART temperature attribute.
5. Assumes system is powered off and ready to be powered on.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.
Products and specifications discussed herein are subject to change by Micron without notice.

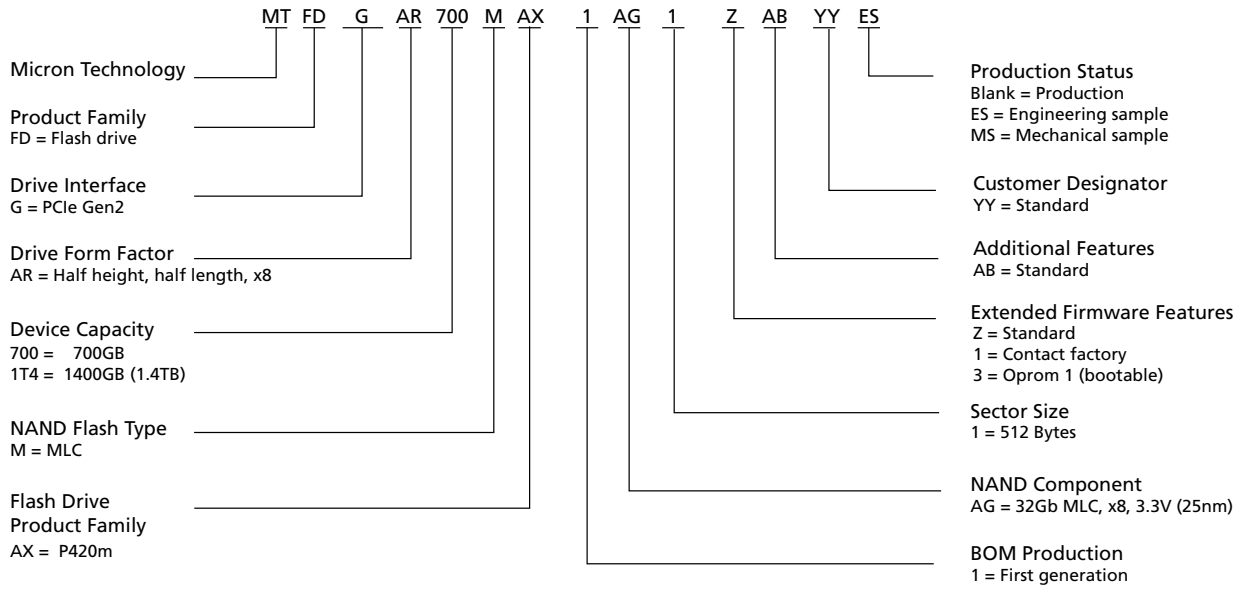
6. Bootable option determined by part number; see Part Numbering Information (page 3). Boot ability may not be compatible with some systems.
7. Power is 30W RMS with power limiting disabled.
8. Varies by capacity. See Performance Specifications (page 5) for details.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Part Numbering Information

The Micron® P420m SSD is available in different configurations and capacities. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

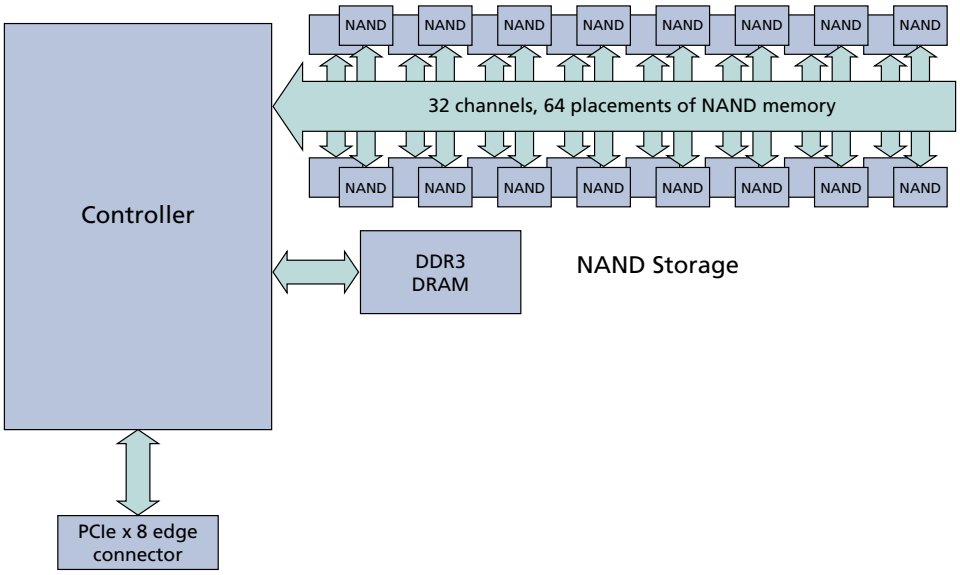
Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

General Description

Micron's P420m SSD is targeted at applications that require high performance and enterprise-class storage reliability. The P420m delivers extremely high IOPS performance due to its ability to support up to 256 outstanding commands while ensuring full end-to-end data protection.

The P420m comes in a half-height, half-length (HHHL) form factor and uses a second-generation (Gen2) PCIe x8 lane interface on the host side and 32 ONFI 2.1-compliant channels on the Flash side.

Figure 2: Functional Block Diagram



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Architecture

The single-chip, Micron-developed ASIC controller, along with the host and Flash interfaces, provide an embedded ATA host bus adapter, a host/Flash translation layer, Flash maintenance, channel control, and Flash RAID (RAIN) protection.

Flash endurance and reliability are optimized through the Flash maintenance features, including static and dynamic wear leveling and RAIN protection. Most of these functions are implemented directly within the controller hardware to optimize performance. The device is shipped in the configurations shown below.

Table 1: Configurations

User Capacity	NAND Flash Process	NAND Flash Density	Package Count	Die per BGA Package
700GB	25nm	32Gb	64	4
1.4TB	25nm	32Gb	64	8

Performance Specifications

Table 2: Performance Specifications

Notes 1–7 apply to entire table

Specification	700GB	1.4TB	Unit
Sequential read	3.3	3.3	GB/s
Sequential write	600	630	MB/s
Random read	750,000	750,000	IOPS
Random write	50,000	95,000	IOPS
Random read/write (70/30) mixed workload	170,000	220,000	IOPS
READ latency	<100 (MIN)	<100 (MIN)	µs
WRITE latency	13 (posted) (MIN)	13 (posted) (MIN)	µs

Notes:
1. Drive is erased and filled with zeroes to achieve preconditioned state.
2. Performance results are with power limiting disabled. Contact Micron for more details regarding performance values with power limiting enabled. Values derived from tests at room temperature.
3. 128KB transfers are used for sequential read/write values; 4KB transfers are used for random read/write values.
4. I/O performance numbers are measured in steady state using FIO with a preconditioned drive under RHEL 6.3 with a queue depth of 256 and with raw device access on systems with a single Intel Xeon E5-2667 2.90 GHz processor with 6 cores, 12 logical and hyper-threading enabled.
5. Steady state performance is defined as conforming to the SNIA V1.0 Performance Test Specification.
6. Latency performance numbers are measured using FIO with queue depth 1, random transfer, 4KB transfer size for READ latency, 4KB transfer size for WRITE latency.
7. Performance numbers are notated in base 10.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Functional Description

Data Retention

Data retention refers to the SSD's media (NAND Flash) capability to retain programmed data when the SSD is powered off. The two primary factors that influence data retention are degree of use (the number of PROGRAM/ERASE cycles on the media) and temperature.

The SSD provides power-off data retention of two months at 40°C (MAX) when total bytes written (TBW) is reached.

Micron RAIN Technology

Redundant array of independent NAND (RAIN) is a technology developed by Micron designed to extend the lifespan of the device.

Residing in the ASIC controller, RAIN is similar to redundant array of independent disks (RAID) technology, but instead of grouping and striping disks, RAIN groups and stripes storage elements on the SSD across multiple channels, generating and storing parity data along with user data (one page of parity for every seven pages of user data). This data structure (user data plus parity) enables complete, transparent data recovery if a single storage element (NAND, page, block, or die) fails. If a failure occurs, the SSD automatically detects it and transparently rebuilds the data. During this RAIN rebuild process, the SSD's performance is reduced temporarily but will recover after the rebuild process completes.

Wear Leveling

Wear leveling is a technique that spreads Flash block use over the entire memory array to equalize the PROGRAM/ERASE cycles on all blocks in the array. This helps to enhance the lifespan of the SSD. The device supports both static and dynamic wear leveling.

Static wear leveling considers all Flash blocks in the SSD regardless of data content or access and maintains an even level of wear across the drive. Dynamic wear leveling monitors available free space on the device and dynamically moves data between Flash blocks to equalize wear on each block. Both techniques are used together within the controller to optimally balance the wear profile of the Flash array, along with the lifespan of the device.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

SMART Attribute Summary

Table 3: SMART Command Reference

Attribute ID	Hex ID	Name	SMART Trip	Description
9	0x09	Power-on hours count	No	Lifetime powered-on hours, from the time the device leaves the factory
12	0x0C	Power cycle count	No	Count of power cycles
170	0xAA	New failing block count	No	Grown defects
171	0xAB	Program fail count	No	Number of NAND program status failures
172	0xAC	Erase fail count	No	Number of NAND erase status failures
174	0xAE	Unexpected power loss count	No	Number of unexpected power-loss occurrences
187	0xBB	Reported uncorrectable errors count	No	Number of ECC correction failures
188	0xBC	Command timeout count	No	Number of command timeouts, defined by an active command being interrupted by a HRESET, COMRESET, SRST, or other command
194	0xC2	Temperature	No	The on-die temperature sensor within the controller ASIC in degrees C, capturing the lifetime high and low temperatures measured
202	0xCA	Percentage of the rated lifetime used	No	Cumulative erase count / lifetime erase count as expressed as a percent. Lifetime erase count is the total number of available blocks * block endurance for the flash technology, read directly from the NAND device.
232	0xE8	Available reserved space	No	Percentage of spare blocks remaining Spare block count
241	0xF1	Power-on (minutes)	No	Lifetime power-on time in minutes
242	0xF2	Write protect progress	No	Progress toward WRITE PROTECT mode: reports 100% when the drive becomes read only
247	0xF7	Cumulative host write sector count	No	Cumulative host program sector count divided by 100,000
248	0xF8	Total NAND pages written count	No	Cumulative program page count divided by 100,000

Note: 1. Attribute/Hex IDs are noted for distribution product. Specific OEMs may have different ID values, but the same list of SMART commands applies.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Logical Block Address Configuration

The number of logical block addresses (LBAs) reported by the P420m ensures sufficient storage space for the specified capacity. Standard LBA settings based on the IDEMA standard (LBA1-02) are shown below.

Table 4: Standard LBA Settings

Capacity	Total LBA		Max LBA		User Available Bytes Unformatted
	Decimal	Hexadecimal	Decimal	Hexadecimal	
700GB	1,367,473,968	5181FF30	1,367,473,967	5181FF2F	700,146,671,616
1.4TB	2,734,926,768	A303ABB0	2,734,926,767	A303ABAF	1,400,282,505,216

Note: 1. 1GB = 1 billion bytes; user capacity.

Physical Configuration

Table 5: Nominal Dimensions and Weight

Specification	Value	Unit
Height	68.90	mm
Width	18.71	mm
Length	167.65	mm
Unit weight with HH bracket	199.59 (700GB) 204.12 (1.4TB)	g
Unit weight with FH bracket	201.85 (700GB) 206.38 (1.4TB)	g

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Interface Connectors

The host interface connector conforms to the PCIe Electromechanical Specification V2.0, section 5, Table 5-1. It is a four-lane, gold-finger connector with 1mm pitch spacing.

A mechanical indent is used to separate the PCIe power pins from the differential signal contacts. The pins are numbered below in ascending order from left to right. Side B refers to component side and Side A refers to the solder side.

Table 6: PCIe Interface Connector Pin Assignments

Pin Number	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12V power	PRSNT1#	Hot Plug Presence Detect
2	+12V	12V power	+12V	12V power
3	+12V	12V power	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	DNU	JTAG2	DNU
6	SMDAT	DNU	JTAG3	DNU
7	GND	Ground	JTAG4	DNU
8	+3.3V	DNU	JTAG5	DNU
9	JTAG1	DNU	+3.3V	DNU
10	3.3Vaux	DNU	+3.3V	DNU
11	WAKE#	DNU	PERST#	PCIe Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	PCIe REFCLK p
14	PETp0	PCIe TX Lane 0 p	REFCLK-	PCIe REFCLK n
15	PETn0	PCIe TX Lane 0 n	GND	Ground
16	GND	Ground	PERp0	PCIe RX Lane 0 p
17	PRSNT2#	Hot Plug Presence Detect	PERn0	PCIe RX Lane 0 n
18	GND	Ground	GND	Ground
19	PETp1	PCIe TX Lane 1 p	RSVD	Reserved
20	PETn1	PCIe TX Lane 1 n	GND	Ground
21	GND	Ground	PERp1	PCIe RX Lane 1 p
22	GND	Ground	PERn1	PCIe RX Lane 1 n
23	PETp2	PCIe TX Lane 2 p	GND	Ground
24	PETn2	PCIe TX Lane 2 n	GND	Ground
25	GND	Ground	PERp2	PCIe RX Lane 2 p
26	GND	Ground	PERn2	PCIe RX Lane 2 n
27	PETp3	PCIe TX Lane 3 p	GND	Ground
28	PETn3	PCIe TX Lane 3 p	GND	Ground
29	GND	Ground	PERp3	PCIe RX Lane 3 p

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

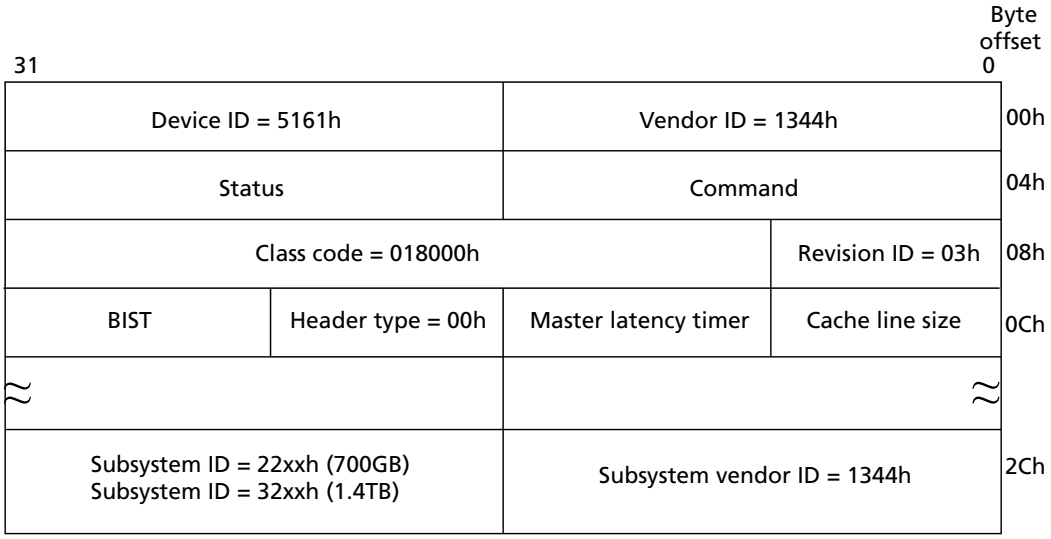
Table 6: PCIe Interface Connector Pin Assignments (Continued)

Pin Number	Side B		Side A	
	Name	Description	Name	Description
30	RSVD	Reserved	PERn3	PCIe RX Lane 3 n
31	PRSNT2#	Hot Plug Presence Detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	PCIe TX Lane 4 p	RSVD	Reserved
34	PETn4	PCIe TX Lane 4 n	GND	Ground
35	GND	Ground	PERp4	PCIe RX Lane 4 p
36	GND	Ground	PERn4	PCIe RX Lane 4 n
37	PETp5	PCIe TX Lane 5 p	GND	Ground
38	PETn5	PCIe TX Lane 5 n	GND	Ground
39	GND	Ground	PERp5	PCIe RX Lane 5 p
40	GND	Ground	PERn5	PCIe RX Lane 5 n
41	PETp6	PCIe TX Lane 6 p	GND	Ground
42	PETn6	PCIe TX Lane 6 n	GND	Ground
43	GND	Ground	PERp6	PCIe RX Lane 6 p
44	GND	Ground	PERn6	PCIe RX Lane 6 n
45	PETp7	PCIe TX Lane 7 p	GND	Ground
46	PETn7	PCIe TX Lane 7 n	GND	Ground
47	GND	Ground	PERp7	PCIe RX Lane 7 p
48	PRSNT2#	Hot Plug Presence Detect	PERn7	PCIe RX Lane 7 n
49	GND	Ground	GND	Ground

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

PCIe Header

Figure 3: PCIe Header



Note: 1. Standard Distribution Subsystem ID is 2200h for 700GB and 3200h for 1.4TB. A non-zero value for xx indicates an OEM product.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Commands

Table 7: Supported ATA Command Set

See ATA–8 ACS–2 specification for command details

Commands	ATA Protocol	CMD Code	Feature Codes
CHECK POWER MODE	ND	0xE5	–
DEVICE CONFIGURATION FREEZE LOCK	ND	0xB1	0xC1
DEVICE CONFIGURATION IDENTIFY	PI	0xB1	0xC2
DEVICE CONFIGURATION RESTORE	ND	0xB1	0xC0
DEVICE CONFIGURATION SET	PO	0xB1	0xC3
DOWNLOAD MICROCODE	PO	0x92	–
EXECUTE DEVICE DIAGNOSTIC	DD	0x90	–
FLUSH CACHE	ND	0xE7	–
FLUSH CACHE EXT	ND	0xEA	–
IDENTIFY DEVICE	PI	0xEC	–
IDLE	ND	0xE3	–
IDLE IMMEDIATE	ND	0xE1	–
INITIALIZE DEVICE PARAMETERS	ND	0x91	–
READ BUFFER	PI	0xE4	–
READ DMA	DM	0xC8	–
READ DMA WO RETRIES	DM	0xC9	–
READ DMA EXT	PI	0x25	–
READ FPMDA QUEUED	NCQ	0x60	–
READ LOG EXT	PI	0x2F	–
READ MULTIPLE	PI	0xC4	–
READ MULTIPLE EXT	PI	0x29	–
READ NATIVE MAX ADDRESS	ND	0xF8	–
READ NATIVE MAX ADDRESS EXT	ND	0x27	–
READ SECTORS	PI	0x20	–
READ SECTORS WO RETRIES	PI	0x21	–
READ SECTORS EXT	PI	0x24	–
READ VERIFY SECTORS	ND	0x40	–
READ VERIFY SECTORS WO RETRIES	ND	0x41	–
READ VERIFY SECTOR EXT	ND	0x42	–
RECALIBRATE	ND	0x1x	–
SECURITY DISABLE PASSWORD	PO	0xF6	–
SECURITY ERASE PREPARE	ND	0xF3	–
SECURITY ERASE UNIT	PO	0xF4	–
SECURITY FREEZE LOCK	ND	0xF5	–
SECURITY SET PASSWORD	PO	0xF1	–
SECURITY UNLOCK	PO	0xF2	–

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Table 7: Supported ATA Command Set (Continued)

See ATA–8 ACS–2 specification for command details

Commands	ATA Protocol	CMD Code	Feature Codes
SEEK	ND	0x7x	–
SET FEATURES	ND	0xEF	VARIOUS
SET MAX ADDRESS	ND	0xF9	0x00
SET NATIVE MAX ADDRESS EXT	ND	0x37	–
SET MAX SET PASSWORD	ND	0xF9	0x01
SET MAX LOCK	ND	0xF9	0x02
SET MAX FREEZE LOCK	ND	0xF9	0x04
SET MAX UNLOCK	ND	0xF9	0x03
SET MULTIPLE MODE	ND	0xC6	–
SLEEP	ND	0xE6	–
SMART DISABLE OPERATIONS	ND	0xB0	0xD9
SMART ENABLE/DISABLE AUTOSAVE	ND	0xB0	0xD2
SMART ENABLE OPERATIONS	ND	0xB0	0xD8
SMART EXECUTE OFF–LINE IMMEDIATE	ND	0xB0	0xD4
SMART READ DATA / READ ATTRIBUTE VALUES	PI	0xB0	0xD0
SMART READ LOG	PI	0xB0	0xD5
SMART RETURN STATUS	ND	0xB0	0xDA
SMART WRITE LOG	PO	0xB0	0xD6
SMART READ ATTRIBUTE/WARRANTY THRESHOLDS	PI	0xB0	0xD1
STANDBY	ND	0xE2	–
STANDBY IMMEDIATE	ND	0xE0	–
WRITE BUFFER	PO	0xE8	–
WRITE DMA	DM	0xCA	–
WRITE DMA WO RETRIES	DM	0xCB	–
WRITE DMA EXT	DM	0x35	–
WRITE DMA FUA EXT	DM	0x3D	–
WRITE FPDMA QUEUED	NCQ	0x61	–
WRITE LOG EXT	PO	0x3F	–
WRITE MULTIPLE	PO	0xC5	–
WRITE MULTIPLE EXT	PO	0x39	–
WRITE MULTIPLE FUA EXT	PO	0xCE	–
WRITE SECTORS	PO	0x30	–
WRITE SECTORS WO RETRIES	PO	0x31	–
WRITE SECTORS EXT	PO	0x34	–

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Reliability

Micron's SSDs incorporate advanced technology for defect and error management. They use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 8: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
1 sector per 10^{17} bits read	READ

Mean Time to Failure

The mean time to failure (MTTF) for the device was measured in a Reliability Demonstration Test at over 2 million hours.

Table 9: MTTF

Capacity	MTTF (Operating Hours)
700GB	2.0 million
1.4TB	

Endurance

Endurance for the device can be predicted based on the usage conditions applied to the device, the internal NAND component PROGRAM/ERASE cycles, the write amplification factor, and the wear-leveling efficiency of the drive. The table below shows the drive lifetime for each SSD capacity based on predefined usage conditions. The SSD implements wear leveling in hardware to optimize performance and efficiency while maintaining Flash endurance.

Table 10: Drive Lifetime

Capacity	Workload [1]	Total Bytes Written	Drive Fills per Day	Retention
700GB	4KB random writes	4.6PB	3.7 (5 years)	2 months
	128KB sequential writes	9.7PB	7.6 (5 years)	2 months
1.4TB	4KB random writes	9.2PB	3.7 (5 years)	2 months
	128KB sequential writes	19.5PB	7.6 (5 years)	2 months

Note: 1. Workloads are 100% writes.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Power Holdup Protection

If power is interrupted at any time while data is being programmed into the NAND, it is possible that data loss may occur and the MLC NAND's lower page may become corrupted. This can cause drive errors to be reported to the host. To prevent these errors from occurring, the device implements an energy storage solution called a power holdup circuit that maintains power to the NAND while it is being programmed, even if power to the system is interrupted. By supporting power holdup, the device ensures that data integrity in the drive is preserved to prevent the loss of data and the reporting of drive errors to the host.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Operating Voltage and Power

Electrical Characteristic	Value
Voltage requirement	+12Vdc (±8%)
Active power (power limiting disabled)	25W RMS (700GB)
	30W RMS (1.4TB)
Active power (power limiting enabled)	25W RMS (1.4TB only)
Standby power (idle)	8W RMS (TYP), 10W RMS (MAX)

Table 12: Environmental Conditions

Temperature and Airflow	Min	Max	Unit	Notes
Operating temperature (as indicated by SMART temperature)	0	85	°C	1
Operating ambient temperature	0	55	°C	2
Storage temperature (in system)	0	40	°C	3
Storage temperature (offline)	–40	85	°C	4
Operating airflow	1.0	–	m/s	5

Notes:
1. If SMART temperature exceeds 85°C, write performance is throttled.
2. Temperature of air impinging on the drive.
3. Assumes system is powered off and ready to be powered on.
4. Contact Micron for additional information.
5. Airflow must flow along the length of the drive, parallel to and through any cooling fins; 1.5m/s operating airflow is recommended.

Table 13: Shock and Vibration

Parameter/Condition	Specification
Shock (nonoperational)	400g at 2ms half-sine 150g at 10ms half-sine
Vibration (nonoperational)	3.1 grms 5–800Hz at 30 min/axis

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Compliance

The device complies with the following specifications:

- RoHS - Restriction of Hazardous Substances
- China RoHS
- WEEE Waste Electric and Electronic Equipment
- Halogen Free - meets IPC low-halogen requirements
- CE (Europe) EN55022/EN55024 (Class A)
- TUV (Germany) EN60950
- UL (US/Canada) EN60950
- FCC (US) 47CFR Part 15 Class A
- BSMI (Taiwan) CNS 13438 Class A
- VCCI (Japan) EN 55022/CISPR 22 Class A
- C-TICK (AUS/NZ) CISPR22
- ICES (Canada) CISPR22 Class A
- KC (Korea) - EN55022/EN55024 Class A, KCC-REM-MU2-MTFDGARXXXMAX

FCC Rules

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

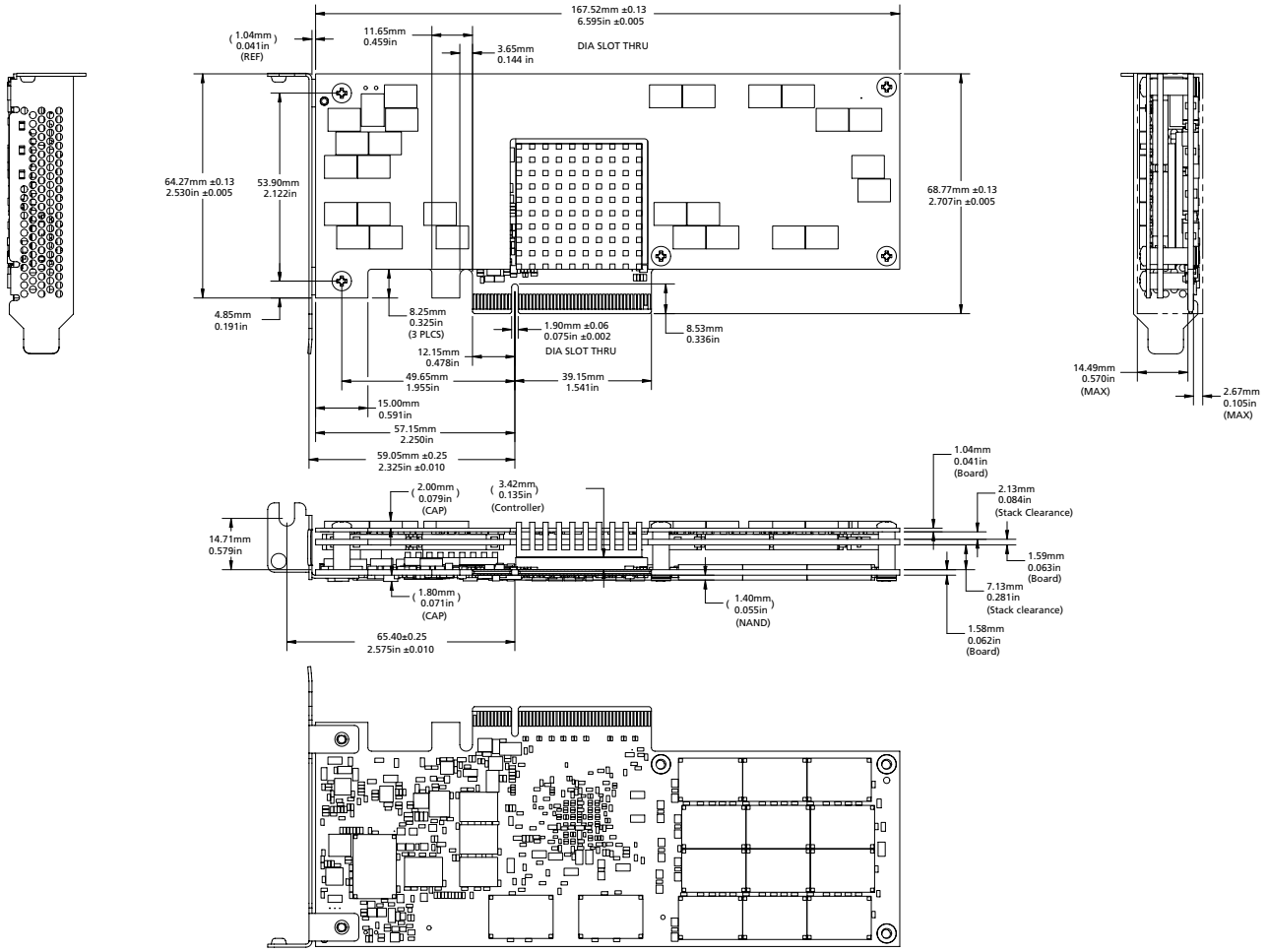
References

- PCI Express Base Specification V2.1
- PCI Express CEM Specification V2.0
- ATA8-ACS2 Specification
- IDEMA Specification
- SNIA Performance Test Specification V1.0

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Drive Dimensions

Figure 4: Half-Height, Half-Length Dimensions



Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Revision History

Rev. O – 08/14

- Updated custom drivers status.

Rev. N – 07/14

- Changed documentation status

Rev. M – 07/14

- Updated custom drivers list

Rev. L – 03/14

- Updated Compliance section

Rev. K – 02/14

- Updated Compliance section

Rev. J – 01/14

- Updated 12V power range

Rev. I – 01/14

- Updated custom drivers list

Rev. H – 12/13

- Status changed to Production
- Updated endurance and data retention specifications
- Updated electrical specifications

Rev. G – 10/13

- Updated temperature specification and notes

Rev. F – 10/13

- Updated custom drivers list
- Updated shock and vibration

Rev. E – 9/13

- Updated custom drivers list

Rev. D – 8/13

- Updated temperature and performance specifications
- Updated custom drivers list

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.

Rev. C – 7/13

- Updated note 3 in Performance Specifications section

Rev. B – 6/13

- Updated performance and latency specifications

Rev. A – 6/13

- Initial release; Preliminary status

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992
Micron and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.
This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Micron Technology, Inc. reserves the right to change products or specifications without notice.
© 2013 Micron Technology, Inc. All rights reserved.